CLAIMS

What is claimed is:

1. A system for monitoring the status of data and components during data packet processing, the system comprising:

a packet processor, wherein the packet processor generates processing data based on one or more control structures while revising packet data, wherein the packet processor generates the processing data while performing one or more lookup cycles; and

a buffer, wherein the buffer records the processing data and the status of the one or more control structures, wherein the processing data includes a lookup number, wherein the lookup number identifies the number of cycles performed by the packet processor.

2. The system for monitoring the status of data and components during data packet processing of claim 1, further comprising:

a trigger status register, wherein the trigger status register is configured to be read by a host processor to provide information regarding the location of stored data in the buffer related to a trigger.

3. The system for monitoring the status of data and components during data packet processing of claim 1, further comprising:

a trigger status register, wherein the trigger status register includes a lookup count and a trigger vector, wherein the lookup count identifies data recorded in the buffer from a first cycle of the packet processor, wherein the trigger vector indicates the number of packet processor slots that met a trigger condition.

4. The system for monitoring the status of data and components during data packet processing of claim 1, further comprising:

a trigger source register, wherein the trigger source register records data identifying the location of trigger data.

5. The system for monitoring the status of data and components during data packet processing of claim 1, further comprising:

a port, wherein a packet header is combined with buffer data, and the packet header and buffer data are made available through the port.

6. The system for monitoring the status of data and components during data packet processing of claim 1, wherein the buffer is incorporated into an integrated circuit with the packet processor and the buffer is configured to be intermittently in communication with a host processor, wherein the host processor is not incorporated into the integrated circuit.

7. The system for monitoring the status of data and components during data packet processing of claim 1, wherein the buffer is a circular buffer.

8. The system for monitoring the status of data and components during data packet processing of claim 1, wherein the buffer is a circular buffer, wherein the circular buffer records processing data and the status of the control structures for a plurality of the lookup cycles.

9. The system for monitoring the status of data and components during data packet processing of claim 1, wherein the buffer is configured to operate with a host processor.

10. The system for monitoring the status of data and components during data packet processing of claim 1, wherein the buffer is configured to operate with a second processor, where the second processor and the buffer are configured to function as a mailbox for a host processor.

11. The system for monitoring the status of data and components during data packet processing of claim 1, wherein the buffer is configured to operate with a host processor, wherein the mailbox is configured to be optionally programmed by the packet processor or the host processor.

12. The system for monitoring the status of data and components during data packet processing of claim 1, wherein data stored in the buffer is provided upon the satisfaction of a trigger condition.

13. The system for monitoring the status of data and components during data packet processing of claim 1, wherein data stored in the buffer is provided to a host processor upon the satisfaction of a trigger condition from a trigger source, wherein the trigger source is one of a group of trigger sources, wherein the group of trigger sources consists of: an ingress port, an SCT index, a CAM match address and flags, an AFH data structure, and a statistics data structure.

14. The system for monitoring the status of data and components during data packet processing of claim 1, wherein data stored in the buffer is provided to a host processor upon the satisfaction of a trigger condition from a plurality of trigger sources, wherein the plurality of trigger sources are associated with masks.

15. The system for monitoring the status of data and components during data packet processing of claim 1, wherein data stored in the buffer includes: a first command index; an ingress port; a lookup number; a SCT index; a CAM command; a CAM key; a context pointer set; page flags; VLAN flags; L3 select flags; a VLAN identifier; a receive associated RAM derived VLAN indication; internal VPST flags; AFH derived VPST flags; a CAM match address; CAM flags; an exception PTI; an exception priority; a revised AFH data structure; and a revised statistics data structure.

16. The system for monitoring the status of data and components during data packet processing of claim 1, wherein the buffer is of a fixed size, and the buffer is overwritten in a wraparound fashion when the data reaches the fixed size of the buffer.

17. The system for monitoring the status of data and components during data packet processing of claim 1, wherein the buffer includes addresses, wherein the addresses consist of a processing slot and a cycle count, wherein the processing slot indicates a packet processor processing slot, wherein the cycle count indicates a packet processor cycle count.

18. The system for monitoring the status of data and components during data packet processing of claim 1, wherein the buffer is configured to operate with a second processor, where the second processor and the buffer are configured to search for data, wherein a user may specify the data searched for.

19. The system for monitoring the status of data and components during data packet processing of claim 1, wherein the packet data being revised is a datagram header.

20. A system for monitoring the status of data and components during data packet processing, the system comprising:

a packet processor, wherein the packet processor generates processing data and while revising packet data based on a packet header modification recipe and the status of one or more control structures; and

a buffer, wherein the buffer records the processing data and the status of the one or more control structures.

21. The system for monitoring the status of data and components during data packet processing of claim 20, further comprising:

a trigger status register, wherein the trigger status register is configured to be read by a host processor to provide information regarding the location of stored data in the buffer related to a trigger.

22. The system for monitoring the status of data and components during data packet processing of claim 20, further comprising:

a trigger status register, wherein the trigger status register includes a trigger vector, wherein the trigger vector indicates the number of packet processor slots that met a trigger condition.

23. The system for monitoring the status of data and components during data packet processing of claim 20, further comprising:

a trigger source register, wherein the trigger source register records data identifying the location of trigger data.

24. The system for monitoring the status of data and components during data packet processing of claim 20, further comprising:

a port, wherein a packet header is combined with buffer data, and the packet header and buffer data are made available through the port.

25. The system for monitoring the status of data and components during data packet processing of claim 20, wherein the buffer is incorporated into an integrated circuit with the packet processor and the buffer is configured to be intermittently in communication with a host processor, wherein the host processor is not incorporated into the integrated circuit.

26. The system for monitoring the status of data and components during data packet processing of claim 20, wherein the buffer is a circular buffer.

27. The system for monitoring the status of data and components during data packet processing of claim 20, wherein the buffer is a circular buffer, wherein the circular buffer records processing data and the status of the control structures for a plurality of processor slots.

28. The system for monitoring the status of data and components during data packet processing of claim 20, wherein the buffer is configured to operate with a host processor.

29. The system for monitoring the status of data and components during data packet processing of claim 20, wherein the buffer is configured to operate with a second processor, where the second processor and the buffer are configured to function as a mailbox for a host processor.

30. The system for monitoring the status of data and components during data packet processing of claim 20, wherein the system is also configured to function as a mailbox for a host processor.

31. The system for monitoring the status of data and components during data packet processing of claim 20, wherein the buffer is configured to operate with a

host processor, wherein the packet processor mailbox is configured to be optionally programmed by the packet processor or the host processor.

32. The system for monitoring the status of data and components during data packet processing of claim 20, wherein data stored in the buffer is provided upon the satisfaction of a trigger condition.

33. The system for monitoring the status of data and components during data packet processing of claim 20, wherein data stored in the buffer is provided to a host processor upon the satisfaction of a trigger condition from a trigger source, wherein the trigger source is one of a group of trigger sources, wherein the group of trigger sources consists of: a transmit modification index; packet data; and the structure of data within an address filtering header.

34. The system for monitoring the status of data and components during data packet processing of claim 20, wherein data stored in the buffer is provided to a host processor upon the satisfaction of a trigger condition from a plurality of trigger sources, wherein the plurality of trigger sources are associated with masks.

35. The system for monitoring the status of data and components during data packet processing of claim 20, wherein data stored in the buffer includes: fragment CAM data; fragment format RAM data; a fragment format RAM address; a transmit work buffer address; data from a transmit work buffer; a context pointer set; transmission engine error flags; the current packet size adjustment; the amount of original egress packet data inside the transmit work buffer; the current packet pointer; the last sequence flag; an address rewind flag; a slush flag; a processor sequence number; and a transmit modification command.

36. The system for monitoring the status of data and components during data packet processing of claim 20, wherein the buffer is of a fixed size, and the buffer is overwritten in a wraparound fashion when the data reaches the fixed size of the buffer.

37. A method for monitoring the status of data and components during data packet processing, the method including the steps of:

generating processing data based on one or more control structures while revising packet data while performing one or more lookup cycles; and

recording the processing data and the status of the one or more control structures, wherein the processing data includes a lookup number, wherein the lookup number identifies the number of cycles performed by the packet processor.

38. The method for monitoring the status of data and components during data packet processing of claim 37, further comprising the step of:

providing information regarding the location of stored data in the buffer related to a trigger.

39. The method for monitoring the status of data and components during data packet processing of claim 37, further comprising the step of:

identifying data recorded in a the buffer from a first cycle of the packet processor.

40. The method for monitoring the status of data and components during data packet processing of claim 37, further comprising the step of:

recording data identifying the location of trigger data.

41. The method for monitoring the status of data and components during data packet processing of claim 37, further comprising the step of:

making a packet header and buffer data available at a port, wherein the packet header is combined with the buffer data.

42. The method for monitoring the status of data and components during data packet processing of claim 37, wherein a buffer records the processing data and the status of the one or more control structures and the buffer is incorporated into an integrated circuit with the packet processor and the buffer is configured to be intermittently in communication with a host processor, wherein the host processor is not incorporated into the integrated circuit.

43. The method for monitoring the status of data and components during data packet processing of claim 37, wherein a buffer records the processing data and the status of the one or more control structures and the buffer is a circular buffer.

44. The method for monitoring the status of data and components during data packet processing of claim 37, wherein a buffer records the processing data and the status of the one or more control structures, wherein the buffer is a circular buffer, and wherein the circular buffer records processing data and the status of the control structures for a plurality of the lookup cycles.

45. The method for monitoring the status of data and components during data packet processing of claim 37, wherein a buffer records the processing data and the status of the one or more control structures, wherein the buffer is a circular buffer, and wherein the circular buffer is configured to operate with a host processor.

46. The method for monitoring the status of data and components during data packet processing of claim 37, wherein a buffer records the processing data and the status of the one or more control structures, wherein the buffer is configured to operate with a host processor, wherein the buffer is configured to operate with a second processor, wherein the second processor may be optionally programmed by the packet processor or the host processor.

47. The method for monitoring the status of data and components during data packet processing of claim 37, wherein a buffer records the processing data and the status of the one or more control structures, wherein the data stored in the buffer is provided upon the satisfaction of a trigger condition.

48. The method for monitoring the status of data and components during data packet processing of claim 37, wherein a buffer records the processing data and the status of the one or more control structures, wherein data stored in the buffer is provided to a host processor upon the satisfaction of a trigger condition from a trigger source, wherein the trigger source is one of a group of trigger sources, wherein the group of trigger sources consists of: an ingress port, an SCT index, a CAM match address and flags, an AFH data structure, and a statistics data structure.

49. The method for monitoring the status of data and components during data packet processing of claim 37, wherein a buffer records the processing data and the status of the one or more control structures, wherein data stored in the buffer is

provided to a host processor upon the satisfaction of a trigger condition from a plurality of trigger sources, wherein the plurality of trigger sources are associated with masks.

50. The method for monitoring the status of data and components during data packet processing of claim 37, wherein a buffer records the processing data and the status of the one or more control structures, wherein data stored in the buffer includes: a first command index; an ingress port; a lookup number; a SCT index; a CAM command; a CAM key; a context pointer set; page flags; VLAN flags; L3 select flags; a VLAN identifier; a receive associated RAM derived VLAN indication; internal VPST flags; AFH derived VPST flags; a CAM match address; CAM flags; an exception PTI; an exception priority; a revised AFH data structure; and a revised statistics data structure.

41. The method for monitoring the status of data and components during data packet processing of claim 37, wherein a buffer records the processing data and the status of the one or more control structures, wherein the buffer is of a fixed size, and the buffer is overwritten in a wraparound fashion when the data reaches the fixed size of the buffer.

52. The method for monitoring the status of data and components during data packet processing of claim 37, wherein a buffer records the processing data and the status of the one or more control structures, wherein the buffer includes addresses, wherein the addresses consist of a processing slot and a cycle count, wherein the processing slot indicates a packet processor processing slot, wherein the cycle count indicates a packet processor cycle count.

53. A system for monitoring the status of data and components during data packet processing, the system including:

means for generating processing data based on one or more control structures while revising packet data while performing one or more lookup cycles; and

means for recording the processing data and the status of the one or more control structures, wherein the processing data includes a lookup number, wherein the lookup number identifies the number of cycles performed by the packet processor.

54. The system for monitoring the status of data and components during data packet processing of claim 53, further comprising:

means for providing information regarding the location of stored data in the buffer related to a trigger.

55. The system for monitoring the status of data and components during data packet processing of claim 53, further comprising:

means for identifying data recorded in a the buffer from a first cycle of the packet processor.

56. The system for monitoring the status of data and components during data packet processing of claim 53, further comprising:

means for recording data identifying the location of trigger data.

57. The system for monitoring the status of data and components during data packet processing of claim 53, further comprising:

means for making a packet header and buffer data available at a port, wherein the packet header is combined with the buffer data.

58. The system for monitoring the status of data and components during data packet processing of claim 53, wherein a buffer records the processing data and the status of the one or more control structures and the buffer is incorporated into an integrated circuit with the packet processor and the buffer is configured to be intermittently in communication with a host processor, wherein the host processor is not incorporated into the integrated circuit.

59. The system for monitoring the status of data and components during data packet processing of claim 53, wherein a buffer records the processing data and the status of the one or more control structures and the buffer is a circular buffer.

60. The system for monitoring the status of data and components during data packet processing of claim 53, wherein a buffer records the processing data and the status of the one or more control structures, wherein the buffer is a circular buffer, and wherein the circular buffer records processing data and the status of the control structures for a plurality of the lookup cycles.

61. The system for monitoring the status of data and components during data packet processing of claim 53, wherein a buffer records the processing data and the status of the one or more control structures, wherein the buffer is a circular buffer, and wherein the circular buffer is configured to operate with a host processor.

62. The system for monitoring the status of data and components during data packet processing of claim 53, wherein a buffer records the processing data and the status of the one or more control structures, wherein the buffer is configured to operate with a host processor, wherein the buffer is configured to operate with a second processor, wherein the second processor may be optionally programmed by the packet processor or the host processor.

63. The system for monitoring the status of data and components during data packet processing of claim 53, wherein a buffer records the processing data and the status of the one or more control structures, wherein the data stored in the buffer is provided upon the satisfaction of a trigger condition.

64. The system for monitoring the status of data and components during data packet processing of claim 53, wherein a buffer records the processing data and the status of the one or more control structures, wherein data stored in the buffer is provided to a host processor upon the satisfaction of a trigger condition from a trigger source, wherein the trigger source is one of a group of trigger sources, wherein the group of trigger sources consists of: an ingress port, an SCT index, a CAM match address and flags, an AFH data structure, and a statistics data structure.

65. The system for monitoring the status of data and components during data packet processing of claim 53, wherein a buffer records the processing data and the status of the one or more control structures, wherein data stored in the buffer is

provided to a host processor upon the satisfaction of a trigger condition from a plurality of trigger sources, wherein the plurality of trigger sources are associated with masks.

66. The system for monitoring the status of data and components during data packet processing of claim 53, wherein a buffer records the processing data and the status of the one or more control structures, wherein data stored in the buffer includes: a first command index; an ingress port; a lookup number; a SCT index; a CAM command; a CAM key; a context pointer set; page flags; VLAN flags; L3 select flags; a VLAN identifier; a receive associated RAM derived VLAN indication; internal VPST flags; AFH derived VPST flags; a CAM match address; CAM flags; an exception PTI; an exception priority; a revised AFH data structure; and a revised statistics data structure.

67. The method for monitoring the status of data and components during data packet processing of claim 53, wherein a buffer records the processing data and the status of the one or more control structures, wherein the buffer is of a fixed size, and the buffer is overwritten in a wraparound fashion when the data reaches the fixed size of the buffer.

68. The method for monitoring the status of data and components during data packet processing of claim 53, wherein a buffer records the processing data and the status of the one or more control structures, wherein the buffer includes addresses, wherein the addresses consist of a processing slot and a cycle count, wherein the processing slot indicates a packet processor processing slot, wherein the cycle count indicates a packet processor cycle count.